



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/672,010	09/25/2003	Hisae Shibuya	16869S-095400US	7689
20350 7590 08/18/2009 TOWNSEND AND TOWNSEND AND CREW, LLP TWO EMBARCADERO CENTER EIGHTH FLOOR SAN FRANCISCO, CA 94111-3834				
EXAMINER				
LIEW, ALEX KOK SOON				
ART UNIT		PAPER NUMBER		
2624				
MAIL DATE		DELIVERY MODE		
08/18/2009		PAPER		

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/672,010

Applicant(s)

SHIBUYA ET AL.

Examiner

ALEX LIEW

Art Unit

2624

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 05 May 2009.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-15 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 10 and 11 is/are allowed.
- 6) ☒ Claim(s) 1-9, 12-15 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-8508)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

1. The amendment filed on 5/5/09 is entered and made of record.

2. **Response to applicant's arguments**

I. The amendments made on claims 1-11, overcomes the U.S.C. 101 rejections

II. On pages 11-12, the applicant stated:

"As described in claim 1, a defect distribution shape classifier is used to classify defects into one of the following specific distribution shape characteristic categories: repeated defects, clustered defects, arc-shaped defects, radial regional defects, line type regional defects, and ring and blob type defects. The defect distribution shape classifier classifies as random any other defects which are not classified under the foregoing categories. As discussed below, *Tobin and Ikeda* are different from claim 1 because the defects are not automatically classified into a distribution shape characteristic category by, for example, a defect distribution shape classifier."

The examiner disagrees;

Ikeda (US pat no 7,068,834) disclose a defect data analysis method comprising the steps of obtaining defect position information positions by inspecting a substrate with an inspection apparatus, wherein the substrate is processed in a process of circuit pattern formation on the substrate (figure 2);

storing the obtained defect position information in memory (see column 2, lines 9-11, viewing the images will give one locations of the defects);

processing the defect position information stored in the memory using a processor (see column 2, lines 11-18, the images are processed for classification);

obtaining the defect position information from the processed substrate from the processed (see figure 11, shows position information of the defects);

classifying defects into one of the plurality of characteristic categories by using a shape classifier and the processed defect position information, wherein the plurality of shape characteristic categories comprises: repeated defects, clustered defects, arc-shaped regional defects, radial regional defects, line type regional defects, ring and blob type regional defects and random defects defect (see figure 1 which shows plurality of shapes, figure 11 shows the variety of classification whether the are white, black elongated or large, there are more than of the same defects, the classification function is read on the shape classifier); and

displaying, on a display screen, the classified distribution of defects, wherein the distribution shape characteristic categories are each displayed using different colors (see figure 11).

Ikeda does not disclose obtaining the distribution of defects. Tobin (US pat no 5,982,920) discloses obtaining the distribution of defects (figure 7). One skilled in the art would include obtaining the distribution of defects because to allow users to determine which rework method is needed more to correct the defects on the wafer to improve the manufacturing quality.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1, 4, 7, 8 and 12 – 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ikeda (US pat no 7,068,834) in view of Tubin (US pat no 5,982,920).

With regards to claim 1, Ikeda disclose a defect data analysis method comprising the steps of obtaining defect position information positions by inspecting a substrate with an inspection apparatus, wherein the substrate is processed in a process of circuit pattern formation on the substrate (figure 2);

storing the obtained defect position information in memory (see column 2, lines 9-11, viewing the images will give one locations of the defects);

processing the defect position information stored in the memory using a processor (see column 2, lines 11-18, the images are processed for classification);

obtaining the defect position information from the processed substrate from the processed (see figure 11, shows position information of the defects);

classifying defects into one of the plurality of characteristic categories by using a shape classifier and the processed defect position information, wherein the plurality of shape characteristic categories comprises: repeated defects, clustered defects, arc-shaped regional defects, radial regional defects, line type regional defects, ring and blob type regional defects and random defects defect (see figure 1 which shows plurality of shapes, figure 11 shows the variety of classification whether the are white, black

elongated or large, there are more than of the same defects, the classification function is read on the shape classifier); and

displaying, on a display screen, the classified distribution of defects, wherein the distribution shape characteristic categories are each displayed using different colors (see figure 11).

Ikeda does not disclose obtaining the distribution of defects. Tobin discloses obtaining the distribution of defects (figure 7). One skilled in the art would include obtaining the distribution of defects because to allow users to determine which rework method is needed more to correct the defects on the wafer to improve the manufacturing quality.

With regards to claim 4, Tubin discloses a defect data analysis method as claimed in claim 1, wherein the defects classified into the arc-shaped regional defects are judged to be scratches generated by chemical and mechanical polishing (see column 4, lines 13 to 16).

With regards to claim 7, see the rationale and rejection for claim 1. In addition, before classifying objects in image to a category, the objects need to be identified first.

With regards to claim 8, Tobin discloses a defect data analysis method as claimed in claim 7, wherein the processing step is realized by displaying the defect information in a wafer map format on the display screen (see figure 1, the image must be display on the computer monitor in order to be printed out).

With regards to claims 12 – 15, see the rationale and rejection for claim 1. In addition, see figure 2 of Tobin for input means, 'Wafermap data'.

3. Claims 2 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ikeda (US pat no 7,068,834) in view of Tubin (US pat no 5,982,920) as applied to claim 1 further in view of Smilansky (US pat no 7,016,526).

With regards to claim 2, Ikeda discloses all of the claim elements / features as discussed above in rejection for claim 1 and incorporated herein by reference and also discloses a defect data analysis method as claimed in claim 1, wherein the arc-shaped regional defects are detected by obtained a center candidate point of the defect distribution from the defect distribution characteristic on the Cartesian coordinates (see column 4, lines 4 to 6, arc shaped defects are radial shapes, the position of the defects are also extracted, column 6, lines 41 to 43, and the distribution is taken in figure 2, 'Distribution statistics'), but fails to disclose extracting the defects from the polar coordinate information. Smilansky discloses extracting the defects from the polar coordinates information on each defect using the center candidate point as an origin (see column 19, lines 27 to 33 and fig 18). It would have been obvious to one having ordinary skill in the art at the time of the invention was made to include extracting the defects from the polar coordinate information because wafers are known to be circular (see Smilansky figure 18, radius and angle), converting data from Cartesian to polar

coordinates ease data computations, where best Cartesian coordinate system represents rectangular space (see figure 18, see rectangular grids).

With regards to claim 9, see the rationale and rejection for claim 2.

4. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ikeda (US pat no 7,068,834) in view of Tubin (US pat no 5,982,920) as applied to claim 1 further in view of Li (US pat no 6,130,959).

Ikeda discloses all of the claim elements / features as discussed above in rejection for claim 1 and incorporated herein by reference, but fails to disclose creating distribution data on polar coordinate space from information on the Cartesian space and extracting the radial regional defects from polar coordinate space. Lid discloses creating distribution data on the polar coordinate space according to the information on the Cartesian coordinate space of the objects (see figure 8, shows specimen points in polar coordinate which is converted from the Cartesian coordinate from figure 7) and extracting the radial regional objects from the distribution data on the polar coordinate space (the specimen points are extracted from using reference data points shown in figure 5 and 6).

One skill in the art would extract objects or data information using polar coordinate because wafers are known to be circular converting data from Cartesian to polar

coordinates ease data computations and does not require coordinate rotation (see Li column 4, lines 45 to 52).

5. Claims 3 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ikeda (US pat no 7,068,834) in view of Tubin (US pat no 5,982,920) as applied to claim 1 further in view of Maruo (US pat no 6,408,105).

With regards to claim 3, Ikeda discloses all of the claim elements / features as discussed above in rejection for claim 1 and incorporated herein by reference, but fails to disclose perpendicular bisectors of straight lines connecting arbitrary two defects among the defects distributed on the processed substrate. Maruo discloses center point is extracted as a point having more intersections of perpendicular bisectors of straight lines connecting arbitrary two points (see figure 5, points are P0 and P2). One skill in the art would connect two arbitrary points because to find the distance between individual defects so information is send to the system or operator and have the system or operator perform corrections on the defect to improve quality inspection.

With regards to claim 6, see the rationale and rejection for claim 3. In addition, figure 6 and 7 of Maruo are the polar coordinate transformed space of figure 5.

Allowable subject matter

With regards to claim 10, the examiner cannot find applicable prior art and / or suggestion disclosing weighting a point where a perpendicular of arbitrary two defects from the wafer map passes according to the distance between the two defects and voting the point onto the xy space and detecting (x,y) corresponding to the maximum value on the voted space in combination with the rest of the limitations of claim 10.

With regards to claim 11, see the rationale and rejection for claim 10.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ALEX LIEW whose telephone number is (571)272-8623 or cell (917)763-1192. The examiner can be reached anytime.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Bella can be reached on (571) 272-7778. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Matthew C Bella/
Supervisory Patent Examiner, Art
Unit 2624

/Alex Liew/
AU2624
8/16/09